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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,423	07/07/2003	Gireesh Shrimali	RAMB-01013US0	7449

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DENIRO/RAMBUS
575 MARKET STREET
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SAN FRANCISCO, CA 94105

EXAMINER	
KANG, SUK JIN	

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/614,423	SHRIMALI ET AL.	
	Examiner	Art Unit	
	Suk Jin Kang	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *14 and 46* is/are withdrawn from consideration.

5)☒ Claim(s) *1-13 and 31-44* is/are allowed.

6)☒ Claim(s) *15-30,45 and 47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 24** is objected to because of the following informalities: on line 13 of claim 24, replace "." with –;-- or --,-- after "value". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 15, 21-25, 27-30, 45, and 47** rejected under 35 U.S.C. 103(a) as being unpatentable over **Ramamurthy et al.** (U.S. Patent Application Publication # 2003/0227926 A1) in view of **Meempat et al.** (U.S. Patent Application Publication # 2003/0227932 A1).

Consider **claim 15**, Ramamurthy et al. discloses a method for scheduling data through a component in a network, the method comprising: allocating egress port bandwidth for each of a plurality of egress ports (107, output port module, figure 1) to various inputs (101, input port module, figure 1)([0068] lines 1-4); assigning credits (308, queue credits, figure 1, [0050] lines 6-14) to each of the various inputs (101, input port module, figure 1) in proportion to a predetermined bandwidth allocation ([0070] lines 1-3) for an egress port (107, output port module, figure 1); when an input requests (306, request generator, figure 3) access to an egress port ([0076] lines 1-4) and the input has at least one credit for the requested egress port, allowing the request to proceed to an arbiter (105, scheduler, figure 1) ([0090] lines 6-10); when an input receives a grant (1005, grant dispenser, figure 6B) of access to a requested egress port from the arbiter ([0079]), decrementing the credits of the input for the egress port by one ([0093]), but may not expressly disclose when an input has zero credits for an egress port, disallowing any requests from the input for the egress port from proceeding to the arbiter and when all of the inputs have zero credits for the egress port, resetting the

credits, comprising reassigning credits to each of the various inputs in proportion to the predetermined bandwidth allocation for the egress port.

However, in the same field of endeavor, Meempat et al. discloses when an input has zero credits for an egress port, disallowing any requests from the input for the egress port from proceeding to the arbiter ([0020], [0021]); and when all of the inputs have zero credits for the egress port, resetting the credits, comprising reassigning credits to each of the various inputs in proportion to the predetermined bandwidth allocation for the egress port ([0053], [0054]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate disallowing requests and resetting inputs with zero credits as taught by Meempat et al. with the method as disclosed by Ramamurthy et al. for the purpose of effectively providing fairness, priority, and quality of service for scheduling.

Consider **claim 21**, and as applied to claim 15, Ramamurthy et al., as modified by Meempat et al., discloses wherein the component comprises a packet switch (figure 1 and 4), and the various inputs comprise a plurality of ingress ports in the packet switch (figure 1, 4, and 5b), and wherein each egress port of the packet switch individually allocates bandwidth among the ingress ports ([0018]).

Consider **claim 22**, and as applied to claim 15, Ramamurthy et al., as modified by Meempat et al., discloses wherein the component comprises an input queued with virtual output queuing ("IQ with VOQ") packet switch with a plurality of ingress ports such that each ingress port of the component comprises a virtual output queue for each

egress port, and wherein the various inputs comprise the virtual output queues (figure 4, [0042]).

Consider **claim 23**, and as applied to claim 15, Ramamurthy et al., as modified by Meempat et al., discloses wherein the component comprises an input queued with virtual output queuing ("IQ with VOQ") packet switch with a plurality of ingress ports such that each ingress port of the component comprises a plurality of virtual output queues, and wherein each of the virtual output queues corresponds to a combination of an egress port and at least one item selected from a group comprising a data class and a data priority (figure 4, [0042], [0049]).

Consider **claim 24**, Ramamurthy et al. discloses an apparatus for scheduling data through a network component, the apparatus comprising: a plurality of component ingress ports (101, input port module, figure 1), each comprising a plurality of ingress port queues (457, VOQ, figure 4); a plurality of ingress port processors (453, network processor, figure 4), each receiving requests for access to multiple component egress ports from the plurality of ingress port queues ([0043], [0090] lines 6-10)), wherein an ingress port processor (101, figure 3) in the plurality of ingress port processors includes, credit update circuitry (308, figure 3) to receive an initial number of credits for each queue, wherein the initial number of credits for a queue corresponds to an allocation of bandwidth by one egress port to one queue ([0050] lines 6-14, [0093]); request processing circuitry (306, request generator, figure 3) coupled to the credit update circuitry and coupled to receive a request from a queue for access to an egress port, wherein the request processing circuitry determines whether to allow the request to

proceed to an arbiter (105, scheduler, figure 1) based on criteria including whether a requesting queue's number of credits is greater than a predetermined saturation value ([0107]), but may not expressly disclose wherein the credit update circuitry reassigns the queue's number of credits to the initial number of credits responsive to the each queue's number of credits being zero.

However, in the same field of endeavor, Meempat et al. discloses wherein the credit update circuitry reassigns the queue's number of credits to the initial number of credits responsive to the each queue's number of credits being zero ([0053], [0054]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate reassigning the queue with credits as taught by Meempat et al. with the apparatus as disclosed by Ramamurthy et al. for the purpose of effectively providing fairness, priority, and quality of service for scheduling.

Consider **claim 25**, Ramamurthy et al. discloses an apparatus for scheduling data through a network component, the apparatus comprising: a plurality of component ingress ports (101, input port module, figure 1), each comprising a plurality of ingress port queues (457, VOQ, figure 4); a plurality of ingress port processors (453, network processor, figure 4), each receiving requests for access to multiple component egress ports from the plurality of ingress port queues ([0043], [0090] lines 6-10)), wherein an ingress port processor (101, figure 3) in the plurality of ingress port processors includes, credit update circuitry (308, figure 3) to receive an initial number of credits for each queue, wherein the initial number of credits for a queue corresponds to an allocation of bandwidth by one egress port to one queue ([0050] lines 6-14, [0093]); request

processing circuitry (306, request generator, figure 3) coupled to the credit update circuitry and coupled to receive a request from a queue for access to an egress port, wherein the request processing circuitry determines whether to allow the request to proceed to an arbiter (105, scheduler, figure 1) based on criteria including whether a requesting queue's number of credits is greater than a predetermined saturation value ([0107]), but may not expressly disclose wherein the apparatus is cooperative with a strict priority scheme that assigns data one of a plurality of priorities, and wherein all data on the ingress ports is assigned a same priority for purposes of determining whether to allow a request to proceed to the arbiter.

However, in the same field of endeavor, Meempat et al. discloses wherein the apparatus is cooperative with a strict priority scheme that assigns data one of a plurality of priorities, and wherein all data on the ingress ports is assigned a same priority for purposes of determining whether to allow a request to proceed to the arbiter ([0088], [0093]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a strict priority scheme assigning a same priority as taught by Meemphat et al. with the apparatus as disclosed by Ramamurthy et al. for the purpose of effectively providing fairness, priority, and quality of service for scheduling.

Consider **claim 27**, and as applied to claim 24, Ramamurthy et al., as modified by Meempat et al., discloses the apparatus further comprising: grant allocation circuitry that receives a grant from the arbiter granting access to an egress port and allocates

the grant to one of a plurality of data classes according to a predetermined allocation scheme (figure 6b, [0136], [0137]); request update circuitry coupled to the grant allocation circuitry to receive the allocated grant and new requests (figure 6b, [0128], [0138], [0139]); and request count circuitry coupled to the request update circuitry to receive the allocated grant and new requests and updating request counts for respective classes of data accordingly (figure 6b, [0138], [0139]).

Consider **claim 28**, and as applied to claim 27, Ramamurthy et al., as modified by Meempat et al., discloses wherein the credit update circuitry is further coupled to receive the allocated grant and, in response, decrement a number of credits for a queue that was allocated the grant ([0138], [0139]).

Consider **claim 29**, and as applied to claim 28, Ramamurthy et al., as modified by Meempat et al., discloses wherein the request processing circuitry is coupled to the credit update circuitry to receive current credit values for all of the queues (figure 5b, [0092]); the request processing circuitry is coupled to the egress ports to send a flow_done signal to each egress port to indicate that all queues for a respective ingress port have exhausted their allocations of that egress port's bandwidth ([0092]); and the request processing circuitry receives an egress_done signal from each egress port indicating that the respective egress port has no pending requests from any ingress ports ([0092], [0126]).

Consider **claim 30**, and as applied to claim 29, Ramamurthy et al., as modified by Meempat et al., discloses wherein the credit update circuitry responds to the

egress_done signal by resetting credits for each queue to the initial number ([0137], [0147]).

Consider **claim 45**, Ramamurthy et al. discloses a method, comprising: assigning a plurality of credit values to each of a respective plurality of inputs in proportion to a predetermined bandwidth allocation for an egress port (107, output port module, figure 1) ([0050] lines 6-14, [0093]); determining whether an input in the plurality of inputs requests (306, request generator, figure 3) access to the egress port ([0076]), [0077]); determining whether a credit value associated with the input is greater than zero ([0084], [0090], [0108]); allowing the request to proceed to an arbiter (105, scheduler, figure 1) responsive to the determining steps ([0049], [0050], [0084]); decrementing the credit value of the input for the egress port responsive to the input receiving a grant of access to the egress port from the arbiter ([0167] lines 10-14); but may not expressly disclose reassigning the plurality of credit values to each of the respective plurality of inputs in proportion to the predetermined bandwidth allocation for the egress port responsive to the plurality of credit values being zero.

However, in the same field of endeavor, Meempat et al. discloses reassigning the plurality of credit values to each of the respective plurality of inputs in proportion to the predetermined bandwidth allocation for the egress port responsive to the plurality of credit values being zero ([0053], [0054]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate reassigning the queue with credits as

taught by Meempat et al. with the apparatus as disclosed by Ramamurthy et al. for the purpose of effectively providing fairness, priority, and quality of service for scheduling.

Consider **claim 47**, and as applied to claim 45, Ramamurthy et al., as modified by Meempat et al., discloses wherein the allowing step further includes allowing the request to proceed when no other inputs have pending requests for the egress port ([0076], [0084]).

4. **Claims 16-20 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ramamurthy et al.** (U.S. Patent Application Publication # 2003/0227926 A1) in view of **Xu et al.** (U.S. Patent # 7,324,452 B2).

Consider **claim 16**, Ramamurthy et al. discloses a method for scheduling data through a component in a network, the method comprising: allocating egress port bandwidth for each of a plurality of egress ports (107, output port module, figure 1) to various inputs (101, input port module, figure 1)([0068] lines 1-4); assigning credits (308, queue credits, figure 1, [0050] lines 6-14) to each of the various inputs (101, input port module, figure 1) in proportion to a predetermined bandwidth allocation ([0070] lines 1-3) for an egress port (107, output port module, figure 1); when an input requests (306, request generator, figure 3) access to an egress port ([0076] lines 1-4) and the input has at least one credit for the requested egress port, allowing the request to proceed to an arbiter (105, scheduler, figure 1) ([0090] lines 6-10); when an input receives a grant (1005, grant dispenser, figure 6B) of access to a requested egress port from the arbiter ([0079]), decrementing the credits of the input for the egress port by one

([0167] lines 10-14), but may not expressly disclose an input has a request for an egress port, the input has credits <= zero for the requested egress port.

However, in the same field of endeavor, Xu et al. discloses an input has a request for an egress port, the input has credits <= zero for the requested egress port (50, figure 4, column 5 lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate input credits that are less than zero as taught by Xu et al. with the apparatus as disclosed by Ramamurthy et al. for the purpose of effectively providing fairness, priority, and quality of service for scheduling.

Consider **claim 17**, and as applied to claim 16, Ramamurthy et al., as modified by Xu et al., discloses the method further comprising considering a priority assignment in allowing a request to proceed to an arbiter, including: assigning a first priority to requests from inputs that have credits >zero for the requested egress port ([0084], [0076]); and assigning a second priority, wherein second priority requests are only granted when no first priority requests are pending ([0084], [0076]), but may not expressly disclose the input has credits <= zero for the requested egress port.

Nonetheless, Xu et al. further discloses the input has credits <= zero for the requested egress port (50, figure 4, column 5 lines 58-67).

Consider **claim 18**; and as applied to claim 16, Ramamurthy et al., as modified by Xu et al., discloses the method further comprising, updating the credits, comprising adding credits in proportion to the predetermined bandwidth allocation to each of the

various inputs ([0093], [0107]), but may not expressly disclose the input has credits <= zero for the requested egress port.

Nonetheless, Xu et al. further discloses the input has credits <= zero for the requested egress port (50, figure 4, column 5 lines 58-67).

Consider **claim 19**, and as applied to claim 16, Ramamurthy et al., as modified by Xu et al., discloses the method further comprising a maximum negative value, wherein the method further comprises, when an input has credits = maximum negative value for an egress port, disallowing any requests from the input for the egress port from proceeding to the arbiter ([0108], [0110]).

Consider **claim 20**, and as applied to claim 19, Ramamurthy et al., as modified by Xu et al., discloses the method further comprising, updating the credits, comprising adding credits to the current credits for each of the various inputs in proportion to the bandwidth allocation for the egress port ([0093], [0107], [0138]), but may not expressly disclose the input has credits <= zero for the requested egress port.

Nonetheless, Xu et al. further discloses the input has credits <= zero for the requested egress port (50, figure 4, column 5 lines 58-67).

Consider **claim 26**, Ramamurthy et al. discloses an apparatus for scheduling data through a network component, the apparatus comprising: a plurality of component ingress ports (101, input port module, figure 1), each comprising a plurality of ingress port queues (457, VOQ, figure 4); a plurality of ingress port processors (453, network processor, figure 4), each receiving requests for access to multiple component egress ports from the plurality of ingress port queues ([0043], [0090] lines 6-10)), wherein an

ingress port processor (101, figure 3) in the plurality of ingress port processors includes, credit update circuitry (308, figure 3) to receive an initial number of credits for each queue, wherein the initial number of credits for a queue corresponds to an allocation of bandwidth by one egress port to one queue ([0050] lines 6-14, [0093]); request processing circuitry (306, request generator, figure 3) coupled to the credit update circuitry and coupled to receive a request from a queue for access to an egress port, wherein the request processing circuitry determines whether to allow the request to proceed to an arbiter (105, scheduler, figure 1) based on criteria including whether a requesting queue's number of credits is greater than a predetermined saturation value ([0107]), wherein the apparatus is cooperative with a strict priority assignment scheme that assigns data one of a plurality of priorities, and wherein all of the data on the ingress ports is initially assigned one priority for purposes of determining whether to allow a request to proceed to the arbiter ([0084]), and the requesting queue is assigned a different priority that is lower than the initially assigned priority, such that the requesting queue's request is allowed to proceed to the arbiter when no other queue with the initially assigned priority has a pending request for the egress port ([0050], [0090]).

However, in the same field of endeavor, Xu et al. discloses when a requesting queue's number of credits is equal to or less than zero (50, figure 4, column 5 lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate input credits that are less than zero as

taught by Xu et al. with the apparatus as disclosed by Ramamurthy et al. for the purpose of effectively providing fairness, priority, and quality of service for scheduling.

Allowable Subject Matter

5. Claims 1-13 and 31-44 are allowed.

Response to Arguments

6. Applicant's arguments with respect to claims 15-30, 45, and 47 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

8. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Suk Jin Kang whose telephone number is (571) 270-1771. The examiner can normally be reached on Monday - Friday 8:00-5:00 EST.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Suk Jin Kang
S.J.K./sjk

February 13, 2008

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